

IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended.) A method for making a semiconductor device comprising:

forming a patterned sacrificial gate electrode layer on a substrate,
wherein the sacrificial gate electrode layer that is covered by a hard mask, and
wherein the hard mask that is covered by an etch stop layer, wherein the
sacrificial gate electrode layer is not covered by a silicide layer;

depositing a silicon nitride layer on the substrate, the etch stop layer, and
on opposite sides of the patterned sacrificial gate electrode layer;

removing the silicon nitride layer from part of the substrate and from the
etch stop layer to form first and second spacers on opposite sides of the
patterned sacrificial gate electrode layer;

forming first and second spacers on opposite sides of the patterned
sacrificial gate electrode layer;

forming silicide layers proximate to the first and second spacers, wherein
the etch stop layer inhibits the formation of a silicide layer on any portion of the
sacrificial gate electrode layer;

removing the patterned sacrificial gate electrode layer to generate a trench that is positioned between the first and second spacers; and

filling at least part of the trench with a metal layer.

2. (Currently amended.) The method of claim 1 wherein the patterned sacrificial gate electrode layer is formed on a patterned first dielectric layer that is formed on the a substrate, and further comprising forming source and drain regions that comprise a the silicide layers next to the first and second spacers, and forming a second dielectric layer on the etch stop layer and the substrate.

3. (Original.) The method of claim 2 wherein the patterned first dielectric layer comprises silicon dioxide, and further comprising removing the

second dielectric layer from the etch stop layer, removing the etch stop layer from the hard mask, and removing the hard mask from the patterned sacrificial gate electrode layer prior to removing the patterned sacrificial gate electrode layer.

4. (Withdrawn.) The method of claim 1 wherein the hard mask comprises silicon nitride, the etch stop layer comprises a material that may be etched at a slower rate than silicon nitride may be etched, and the patterned sacrificial gate electrode layer comprises polysilicon, and further comprising removing the patterned first dielectric layer after the patterned sacrificial gate electrode layer is removed.

5. (Withdrawn.) The method of claim 4 wherein the etch stop layer comprises a material that is selected from the group consisting of silicon, silicon dioxide, a metal carbide, a carbon doped silicon nitride, and a metal oxide, and further comprising forming a high-k dielectric layer on the substrate at the bottom of the trench after removing the patterned first dielectric layer, and forming the metal layer on the high-k dielectric layer.

6. (Withdrawn.) The method of claim 5 wherein the high-k dielectric layer comprises a material that is selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate.

7. (Original.) The method of claim 1 wherein the metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, a metal carbide, ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

8. (Original.) The method of claim 7 wherein the metal layer comprises a material that is selected from the group consisting of hafnium,

zirconium, titanium, tantalum, aluminum, and a metal carbide, and has a workfunction that is between about 3.9 eV and about 4.2 eV.

9. (Original.) The method of claim 7 wherein the metal layer comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and has a workfunction that is between about 4.9 eV and about 5.2 eV.

10. Canceled.

11. (Original.) A method for making a semiconductor device comprising:

- forming a first dielectric layer on a substrate;
- forming a polysilicon containing layer on the first dielectric layer;
- forming a first silicon nitride layer on the polysilicon containing layer;
- forming an etch stop layer on the first silicon nitride layer;
- etching the etch stop layer, the first silicon nitride layer, the polysilicon containing layer, and the first dielectric layer, to form a patterned etch stop layer, a patterned first silicon nitride layer, a patterned polysilicon containing layer, and a patterned first dielectric layer;

- depositing a second silicon nitride layer on the substrate, the patterned etch stop layer, and on opposite sides of the patterned polysilicon containing layer;

- removing the second silicon nitride layer from part of the substrate and from the patterned etch stop layer to form first and second spacers on opposite sides of the patterned polysilicon containing layer;

- forming source and drain regions that comprise a silicide next to the first and second spacers;

- forming a second dielectric layer on the patterned etch stop layer and on the substrate;

- removing the second dielectric layer from the patterned etch stop layer;

- removing the patterned etch stop layer from the patterned first silicon nitride layer;

removing the patterned first silicon nitride layer from the patterned polysilicon containing layer;

removing the patterned polysilicon containing layer to generate a trench that is positioned between the first and second spacers; and

filling at least part of the trench with a metal layer.

12. (Withdrawn.) The method of claim 11 wherein the first dielectric layer comprises silicon dioxide and the etch stop layer comprises a material that is selected from the group consisting of silicon, silicon dioxide, a metal carbide, a carbon doped silicon nitride, and a metal oxide, and further comprising removing the patterned first dielectric layer after the patterned polysilicon containing layer is removed.

13. (Withdrawn.) The method of claim 12 further comprising forming a high-k dielectric layer on the substrate at the bottom of the trench after removing the patterned first dielectric layer, and forming the metal layer on the high-k dielectric layer.

14. (Withdrawn.) The method of claim 13 wherein:

the high-k dielectric layer is formed by atomic layer chemical vapor deposition, and comprises a material that is selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate; and

the metal layer fills the entire trench and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, a metal carbide, ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

15. (Original.) The method of claim 11 wherein:

the first dielectric layer is between about 5 and about 20 angstroms thick; the polysilicon containing layer is between about 100 and about 2,000

angstroms thick;

the first silicon nitride layer is between about 100 and about 500 angstroms thick;

the etch stop layer is between about 200 and about 1,200 angstroms thick; and

the metal layer serves as a workfunction metal that fills only part of the trench and is between about 50 and about 1,000 angstroms thick; and

further comprising depositing on the metal layer a trench fill material.

16. (Withdrawn.) A method for making a semiconductor device comprising:

forming a silicon dioxide layer that is between about 5 and about 20 angstroms thick on a substrate;

forming a polysilicon containing layer that is between about 100 and about 2,000 angstroms thick on the silicon dioxide layer;

forming a first silicon nitride layer that is between about 100 and about 500 angstroms thick on the polysilicon containing layer;

forming an etch stop layer that is between about 200 and about 1,200 angstroms thick on the first silicon nitride layer;

etching the etch stop layer, the first silicon nitride layer, the polysilicon containing layer, and the silicon dioxide layer, to form a patterned etch stop layer, a patterned first silicon nitride layer, a patterned polysilicon containing layer, and a patterned silicon dioxide layer;

depositing a second silicon nitride layer on the substrate, the patterned etch stop layer, and on opposite sides of the patterned polysilicon containing layer;

removing the second silicon nitride layer from part of the substrate and from the patterned etch stop layer to form first and second spacers on opposite sides of the patterned polysilicon containing layer;

forming source and drain regions that comprise a silicide next to the first and second spacers;

forming a dielectric layer on the patterned etch stop layer and on the

substrate;

removing the dielectric layer from the patterned etch stop layer;
removing the patterned etch stop layer from the patterned first silicon nitride layer;

removing the patterned first silicon nitride layer from the patterned polysilicon containing layer;

removing the patterned polysilicon containing layer and the patterned silicon dioxide layer to generate a trench that is positioned between the first and second spacers;

forming a high-k dielectric layer on the substrate at the bottom of the trench; and

forming a metal layer on the high-k dielectric layer.

17. (Withdrawn.) The method of claim 16 wherein:

the etch stop layer comprises a material that is selected from the group consisting of silicon, silicon dioxide, a silicon carbide, a carbon doped silicon nitride, and a metal oxide;

the high-k dielectric layer comprises a material that is selected from the group consisting of hafnium oxide, hafnium silicon oxide, lanthanum oxide, zirconium oxide, zirconium silicon oxide, tantalum oxide, barium strontium titanium oxide, barium titanium oxide, strontium titanium oxide, yttrium oxide, aluminum oxide, lead scandium tantalum oxide, and lead zinc niobate; and

the metal layer fills the entire trench and comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, a metal carbide, ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide.

18. (Withdrawn.) The method of claim 17 wherein the metal layer comprises a material that is selected from the group consisting of hafnium, zirconium, titanium, tantalum, aluminum, and a metal carbide, and has a workfunction that is between about 3.9 eV and about 4.2 eV.

19. (Withdrawn.) The method of claim 17 wherein the metal layer comprises a material that is selected from the group consisting of ruthenium, palladium, platinum, cobalt, nickel, and a conductive metal oxide, and has a workfunction that is between about 4.9 eV and about 5.2 eV.

20. (Withdrawn.) The method of claim 16 wherein:

a chemical mechanical polishing process is used to remove the dielectric layer from the patterned etch stop layer, to remove the patterned etch stop layer from the patterned first silicon nitride layer, and to remove the patterned first silicon nitride layer from the patterned polysilicon containing layer; and

the metal layer serves as a workfunction metal that fills only part of the trench and is between about 50 and about 1,000 angstroms thick; and

further comprising depositing on the metal layer a trench fill metal that is selected from the group consisting of tungsten and aluminum.